

THC63LVDF84B/THC63LVDF64B

LVDS 24Bit/18Bit COLOR HOST-LCD PANEL INTERFACE RECEIVER

General Description

The THC63LVDF84B/THC63LVDF64B receiver supports wide VCC range(2.5~3.6V). At single 2.5V supply, the THC63LVDF84B/THC63LVDF64B reduces EMI and power consumption.

The THC63LVDF84B receiver convert the four LVDS(Low Voltage Differential Signaling) data streams back into 28bits of CMOS/TTL data with falling edge clock.

At a transmit clock frequency of 85MHz, 28bits of RGB data and 4bits of LCD timing and control data (HSYNC, VSYNC, CNTL1, CNTL2) are transmitted at a rate of 2.3Gbps.

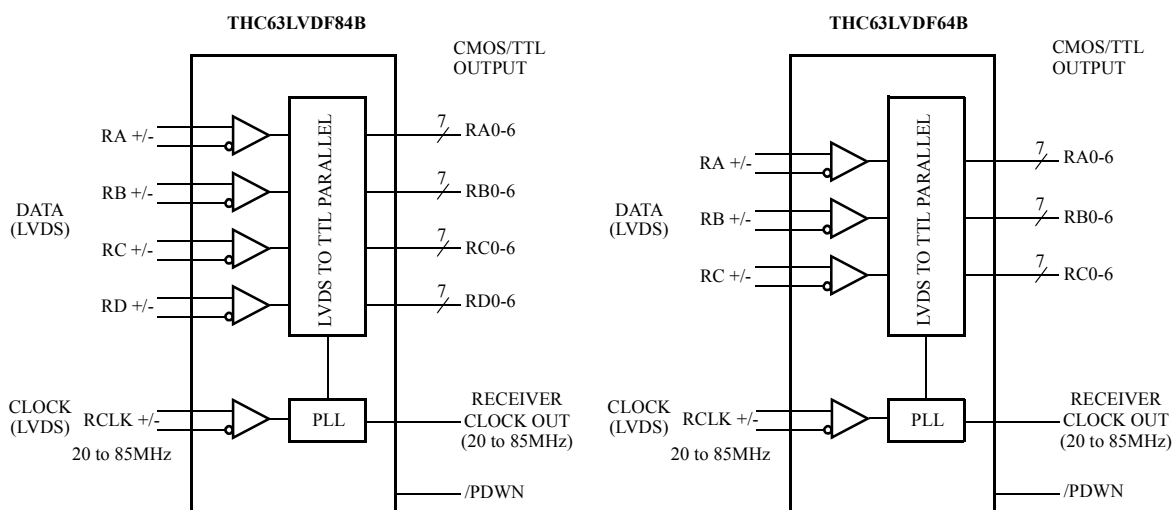
Also the THC63LVDF64B receiver convert the three LVDS data streams back into 21bits of CMOS/TTL data with falling edge clock.

At a transmit clock frequency of 85MHz, 21bits of RGB data and 4bits of LCD timing and control data (HSYNC, VSYNC, CNTL1, CNTL2) are transmitted at a rate of 1.78Gbps.

Features

- Wide VCC range: 2.5~3.6V
- Wide dot clock range: 20-85MHz suited for VGA, SVGA, XGA and SXGA (VCC=3.0~3.6V)
- Wide dot clock range: 20-70MHz suited for VGA, SVGA, XGA and SXGA (VCC=2.5V~3.6V)
- PLL requires No external components
- Rx power consumption < 80mW @VCC 2.5V, 65MHz Grayscale
- Power-Down Mode
- Low profile 56 Lead or 48 Lead TSSOP Package
- Pin compatible with THC63LVDF84A/F64A

Block Diagram



(140-595Mbit/On Each LVDS Channel)

Pin Out

THC63LVDF84B	
RC3	1
RD6	2
RC4	3
GND	4
RC5	5
RC6	6
RD0	7
LVDSGND	8
RA-	9
RA+	10
RB-	11
RB+	12
LVDSVCC	13
LVDSGND	14
RC-	15
RC+	16
RCLK-	17
RCLK+	18
RD-	19
RD+	20
LVDSGND	21
PLLGND	22
PLLVCC	23
PLLGND	24
/PDWN	25
CLKOUT	26
RA0	27
GND	28
	29
	30
	31
	32
	33
	34
	35
	36
	37
	38
	39
	40
	41
	42
	43
	44
	45
	46
	47
	48
	49
	50
	51
	52
	53
	54
	55
	56
VCC	56
RC2	55
RC1	54
RC0	53
GND	52
RB6	51
RD5	50
RD4	49
VCC	48
RB5	47
RB4	46
RB3	45
GND	44
RB2	43
RD3	42
RD2	41
VCC	40
RB1	39
RB0	38
RA6	37
GND	36
RA5	35
RD1	34
RA4	33
RA3	32
VCC	31
RA2	30
RA1	29

THC63LVDF64B	
RC3	1
RC4	2
GND	3
RC5	4
RC6	5
N/C	6
LVDSGND	7
RA-	8
RA+	9
RB-	10
RB+	11
LVDSVCC	12
LVDSGND	13
RC-	14
RC+	15
RCLK-	16
RCLK+	17
LVDSGND	18
PLLGND	19
PLLVCC	20
PLLGND	21
/PDWN	22
CLKOUT	23
RA0	24
	25
	26
	27
	28
	29
	30
	31
	32
	33
	34
	35
	36
	37
	38
	39
	40
	41
	42
	43
	44
	45
	46
	47
	48
VCC	48
RC2	47
RC1	46
RC0	45
GND	44
RB6	43
VCC	42
RB5	41
RB4	40
RB3	39
GND	38
RB2	37
VCC	36
RB1	35
RB0	34
RA6	33
GND	32
RA5	31
RA4	30
RA3	29
VCC	28
RA2	27
RA1	26
GND	25

THC63LVDF84B Pin Description

Pin Name	Pin #	Type	Description
RA+, RA-	9, 10	LVDS IN	LVDS Data Inputs
RB+, RB-	11, 12	LVDS IN	
RC+, RC-	15, 16	LVDS IN	
RD+, RD-	19, 20	LVDS IN	
RCLK+, RCLK-	17, 18	LVDS IN	LVDS Clock Inputs
RA0~RA6	27,29,30,32,33,35,37	OUT	Pixel Data Outputs
RB0~RB6	38,39,43,45,46,47,51	OUT	
RC0~RC6	53,54,55,1,3,5,6	OUT	
RD0~RD6	7,34,41,42,49,50,2	OUT	
CLKOUT	26	OUT	Pixel Clock Output
/PDWN	25	IN	H: Normal operation L: Power down (all outputs are pulled to ground)
VCC	31,40,48,56	Power	Power Supply Pins for TTL outputs and digital circuitry
GND	4,28,36,44,52	Ground	Ground Pins for TTL outputs and digital circuitry
LVDSVCC	13	Power	Power Supply Pin for LVDS inputs
LVDSGND	8,14,21	Ground	Ground Pins for LVDS inputs
PLLVCC	23	Power	Power Supply Pin for PLL circuitry
PLLGND	22,24	Ground	Ground Pins for PLL circuitry

THC63LVDF64B Pin Description

Pin name	Pin #	Type	Description
RA+, RA-	8,9	LVDS IN	LVDS Data Inputs
RB+, RB-	10,11	LVDS IN	
RC+, RC-	14,15	LVDS IN	
RCLK+, RCLK-	16,17	LVDS IN	LVDS Clock Inputs
RA0~RA6	24,26,27,29,30,31,33	OUT	Pixel Data Outputs
RB0~RB6	34,35,37,39,40,41,43	OUT	
RC0~RC6	45,46,47,1,2,4,5	OUT	
CLKOUT	23	OUT	Pixel Clock Output
/PDWN	22	IN	H: Normal operation L: Power down (all outputs are pulled to ground)
VCC	28,36,42,48	Power	Power Supply Pins for TTL outputs and digital circuitry
GND	3,25,32,38,44	Ground	Ground Pins for TTL outputs and digital circuitry
LVDSVCC	12	Power	Power Supply Pin for LVDS inputs
LVDSGND	7,13,18	Ground	Ground Pins for LVDS inputs
PLLVCC	20	Power	Power Supply Pin for PLL circuitry
PLLGND	19,21	Ground	Ground Pins for PLL circuitry

Electrical Characteristics

CMOS/TTL DC SPECIFICATIONS

 $V_{CC} = 2.5V \sim 3.6V, T_a = -10^{\circ}C \sim +70^{\circ}C$

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{IH}	High Level Input Voltage		2.0		VCC	V
V_{IL}	Low Level Input Voltage		GND		0.8	V
V_{OH1}	High Level Output Voltage	VCC= 3.0V ~ 3.6V $I_{OH} = -4mA$	2.4			V
V_{OL1}	Low Level Output Voltage	VCC = 3.0V ~ 3.6V $I_{OL} = 4mA$			0.4	V
V_{OH2}	High Level Output Voltage	VCC= 2.5V ~ 3.0V $I_{OH} = -2mA$	2.1			V
V_{OL2}	Low Level Output Voltage	VCC = 2.5V ~ 3.0V $I_{OL} = 2mA$			0.4	V
I_{IN}	Input Current	0V \leq VIN \leq VCC			± 10	μA

LVDS RECEIVER DC SPECIFICATIONS

 $V_{CC} = 2.5V \sim 3.6V, T_a = -10^{\circ}C \sim +70^{\circ}C$

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{TH}	Differential Input High Threshold	VOC = +1.2V			100	mV
V_{TL}	Differential Input Low Threshold		-100			mV
I_{IN}	Input Current	$V_{IN} = +2.4V/0V$ VCC = 3.6V			± 10	μA

Absolute Maximum Ratings¹

Supply Voltage (Vcc)	-0.3 to +4V
CMOS/TTL Input Voltage	-0.3 to (Vcc + 0.3V)
CMOS/TTL Output Voltage	-0.3V to (Vcc + 0.3V)
LVDS Receiver Input Voltage	-0.3V to (Vcc + 0.3V)
Junction Temperature	+125°C
Storage Temperature Range	-55°C to +150°C
Resistance to soldering heat	+260°C/10sec
Maximum Power Dissipation@25°C	0.5W

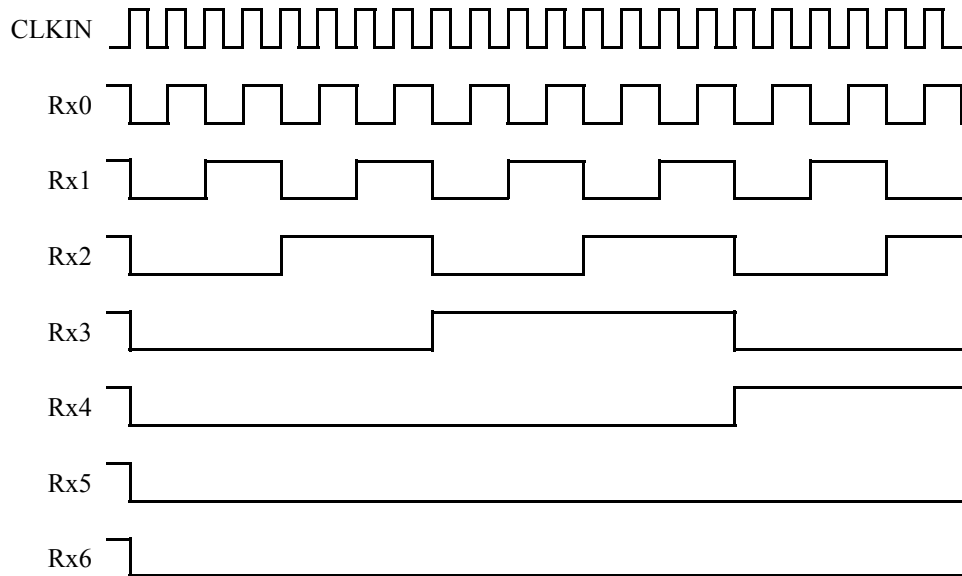
1. "Absolute Maximum Ratings" are those valued beyond which the safety of the device can not be guaranteed. They are not meant to imply that the device should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.

Supply Current

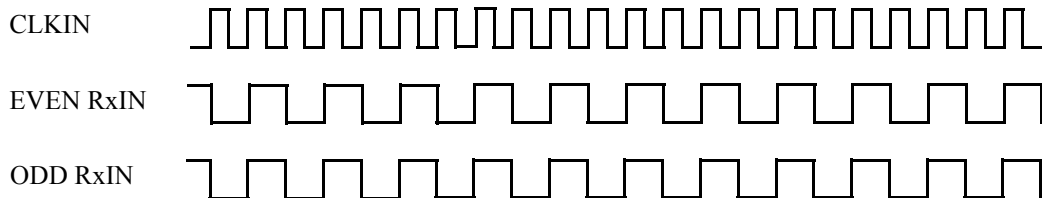
VCC = 2.5V ~ 3.6V, Ta = -10°C ~ +70°C

Symbol	Parameter	Condition(*)		Typ.	Max.	Units
I _{RCCG}	Receiver Supply Current 16Grayscale Pattern	CL=8pF, VCC=3.3V	f = 65MHz	41	53	mA
			f = 85MHz	52	64	mA
		CL=8pF, VCC=2.5V	f = 65MHz	30	42	mA
I _{RCCW}	Receiver Supply Current Worst Case Pattern	CL=8pF, VCC=3.3V	f = 65MHz	72	94	mA
			f = 85MHz	84	96	mA
		CL=8pF, VCC=2.5V	f = 65MHz	42	64	mA
I _{RCCS}	Receiver Power Down Supply Current	/PDWN = L			10	μA

16 Gray Scale Pattern



Worst Case Pattern



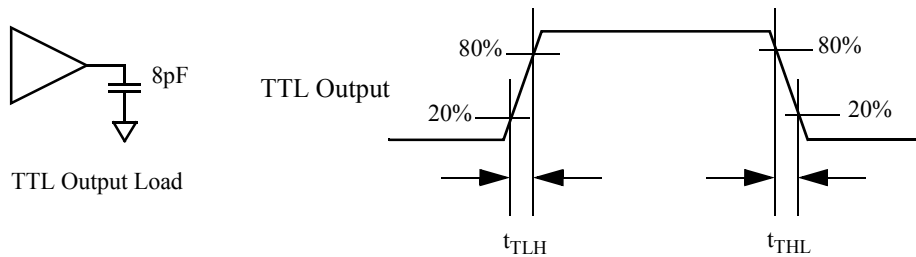
Switching Characteristics

VCC= 2.5V ~ 3.6V, Ta = -10°C ~ +70°C

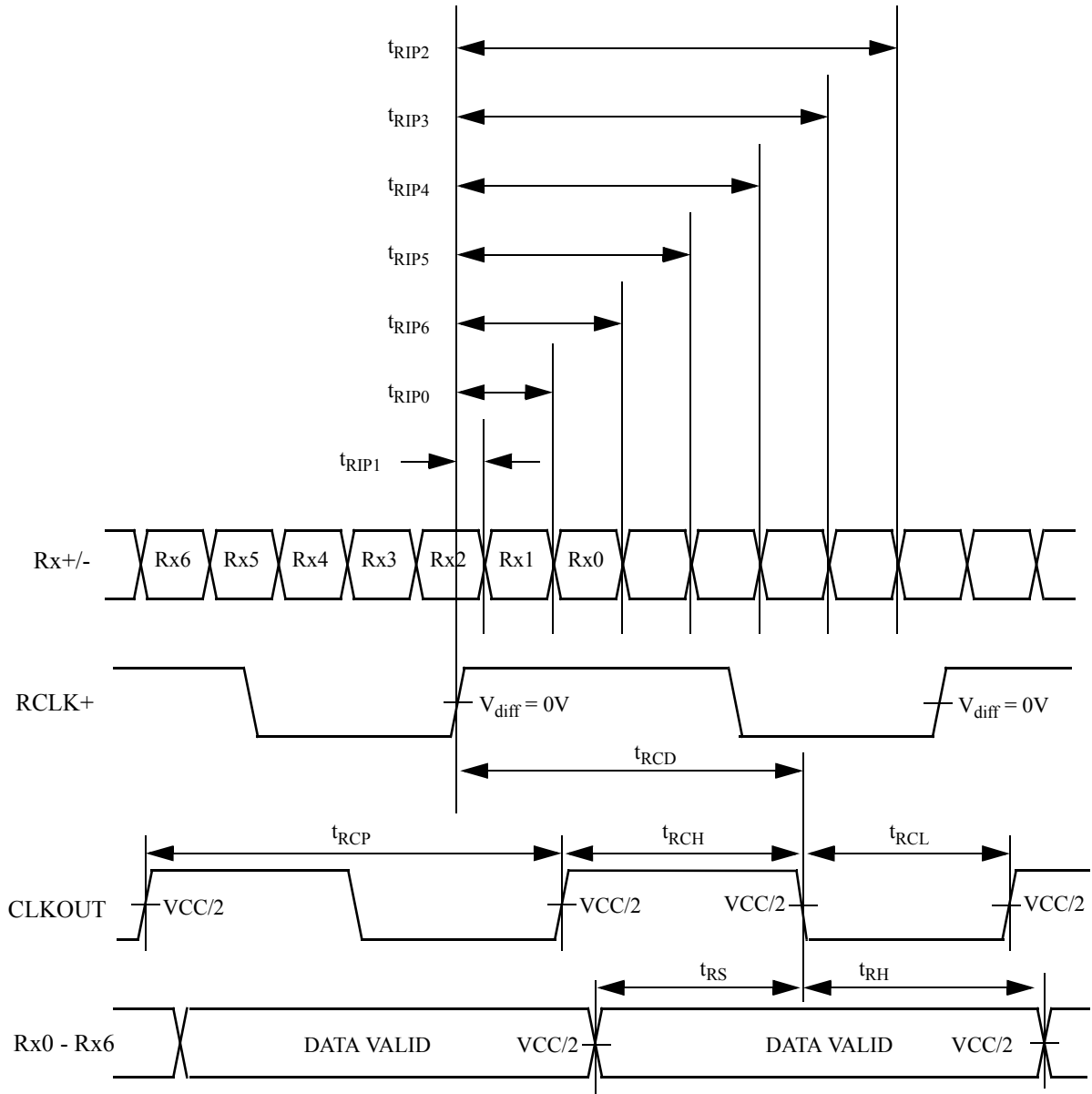
Symbol	Parameter	Min.	Typ.	Max.	Units	
t _{RCP}	CLK OUT Period	VCC = 3.0 - 3.6V	11.76	T	50.0	ns
		VCC = 2.5 - 3.6V	14.28	T	50.0	ns
t _{RCH}	CLK OUT High Time		4T/7		ns	
t _{RCL}	CLK OUT Low Time		3T/7		ns	
t _{RCD}	RCLK +/- to CLK OUT Delay		5T/7		ns	
t _{RS}	TTL Data Setup to CLK OUT	0.35T-0.3			ns	
t _{RH}	TTL Data Hold from CKL OUT	0.45T-1.6			ns	
t _{TLH}	TTL Low to High Transition Time		2.0	3.0	ns	
t _{THL}	TTL High to Low Transition Time		1.8	3.0	ns	
t _{RIP1}	Input Data Position0 (T = 11.76ns)	-0.4	0.0	0.4	ns	
t _{RIP0}	Input Data Position1 (T = 11.76ns)	T/7-0.4	T/7	T/7+0.4	ns	
t _{RIP6}	Input Data Position2 (T = 11.76ns)	2T/7-0.4	2T/7	2T/7+0.4	ns	
t _{RIP5}	Input Data Position3 (T = 11.76ns)	3T/7-0.4	3T/7	3T/7+0.4	ns	
t _{RIP4}	Input Data Position4 (T = 11.76ns)	4T/7-0.4	4T/7	4T/7+0.4	ns	
t _{RIP3}	Input Data Position5 (T = 11.76ns)	5T/7-0.4	5T/7	5T/7+0.4	ns	
t _{RIP2}	Input Data Position6 (T = 11.76ns)	6T/7-0.4	6T/7	6T/7+0.4	ns	
t _{RPLL}	Phase Lock Loop Set			10.0	ms	

AC Timing Diagrams

TTL Output



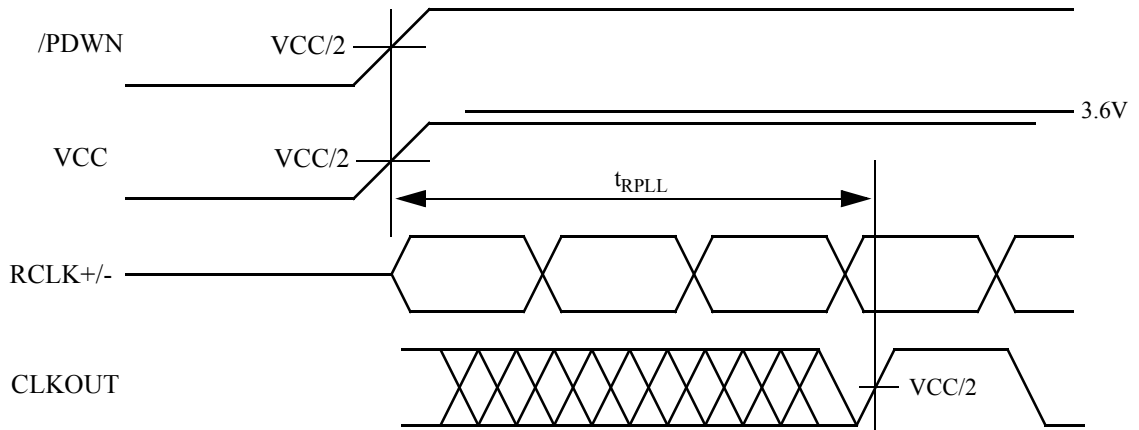
AC Timing Diagrams



Note:
 1) $V_{diff} = (RA+) - (RA-), \dots, (RCLK+) - (RCLK-)$

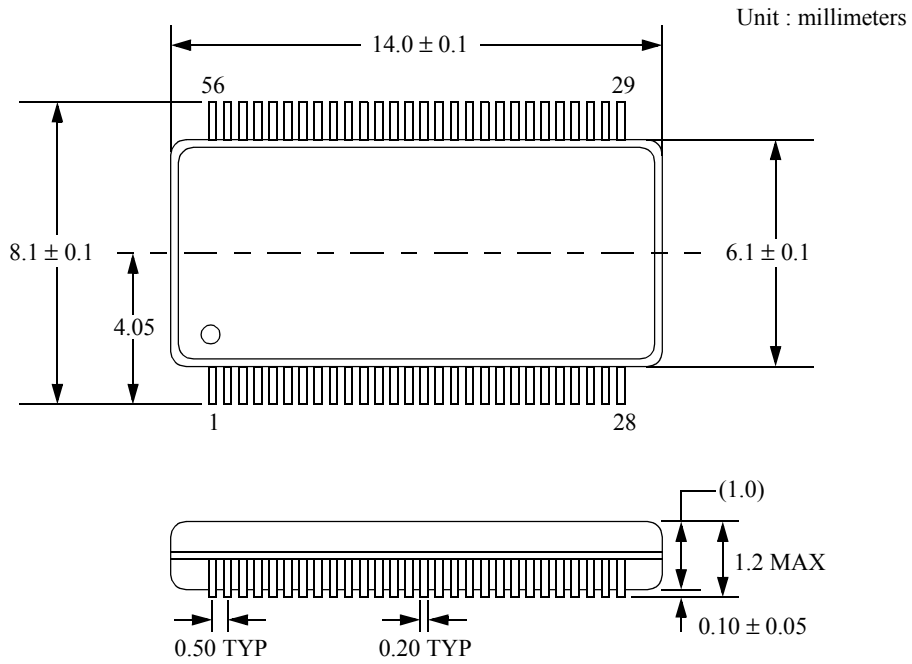
AC Timing Diagrams

Phase Lock Loop Set Time

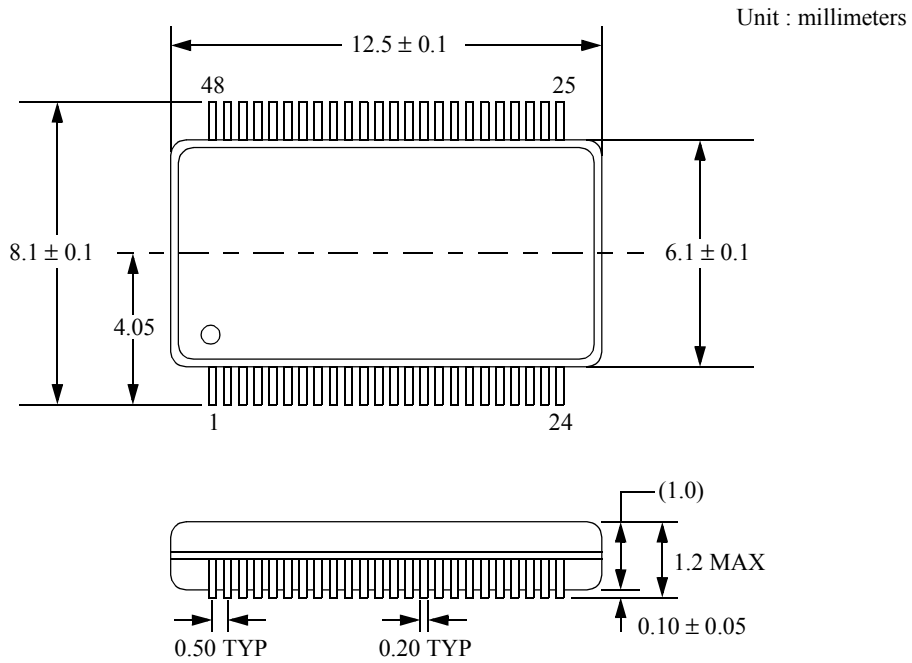


Package

56 Lead Molded Thin Shrink Small Outline Package, JEDEC



48 Lead Molded Thin Shrink Small Outline Package, JEDEC



Notes to Users:

1. The contents of this data sheet are subject to change without prior notice.
2. Circuit diagrams shown in this data sheet are examples of application. Therefore, please pay sufficient attention when designing circuits. Even if there are incorrect descriptions, we are not responsible for any problem due to them. Please note that incorrect descriptions sometimes cannot be corrected immediately if found.
3. Our copyright and know-how are included in this data sheet. Duplication of the data sheet and disclosure to other persons are strictly prohibited without our permission.
4. We are not responsible for any problems of industrial proprietorship occurring during THC63LVDF84B/THC63LVDF64B use, except for those directly related to THC63LVDF84B/THC63LVDF64B's structure, manufacture or functions. THC63LVDF84B/THC63LVDF64B is designed on the premise that it should be used for ordinary electronic devices. Therefore, it shall not be used for applications that require extremely high-reliability (space equipment, nuclear control equipment, medical equipment that affects people's lives, etc.). In addition, when using THC63LVDF84B/THC63LVDF64B for traffic signals, safety devices and control/safety units in transportation equipment, etc., appropriate measures should be taken.
5. We are making the utmost effort to improve the quality and reliability of our products. However, there is a very slight possibility of failure in semiconductor devices. To avoid damage to social or official organizations, much care should be taken to provide sufficient redundancy and fail-safe design.
6. No radiation-hardened design is incorporated in THC63LVDF84B/THC63LVDF64B.
7. Judgment on whether THC63LVDF84B/THC63LVDF64B comes under strategic products prescribed by the Foreign Exchange and Foreign Trade Control Law is the user's responsibility.
8. This technical document was provisionally created during development of THC63LVDF84B/THC63LVDF64B, so there is a possibility of differences between it and the product's final specifications. When designing circuits using THC63LVDF84B/THC63LVDF64B, be sure to refer to the final technical documents.

THine Electronics, Inc.

Wakamatsu Bldg, 6F
3-3-6, Nihombashi-Honcho,
Chuo-ku, Tokyo, 103-0023 Japan
Tel: 81-3-3270-0666
Fax: 81-3-3270-0688